Memory Guide

Cisco Unified Edge M8 Compute Node Memory guide

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Introduction

The Cisco Unified Edge M8 Compute Node Memory guide provides the detailed specifications of the M8 memory DIMMs including:

- Memory DIMMs features
- Cisco PID’s description
- Memory DIMMs guidelines, mixing rules and populations
- All M8 supported DIMM configurations

The Cisco Unified Edge M8 Compute Node Memory guide document applies to the Cisco Unified Edge M8 Compute Node generation server.

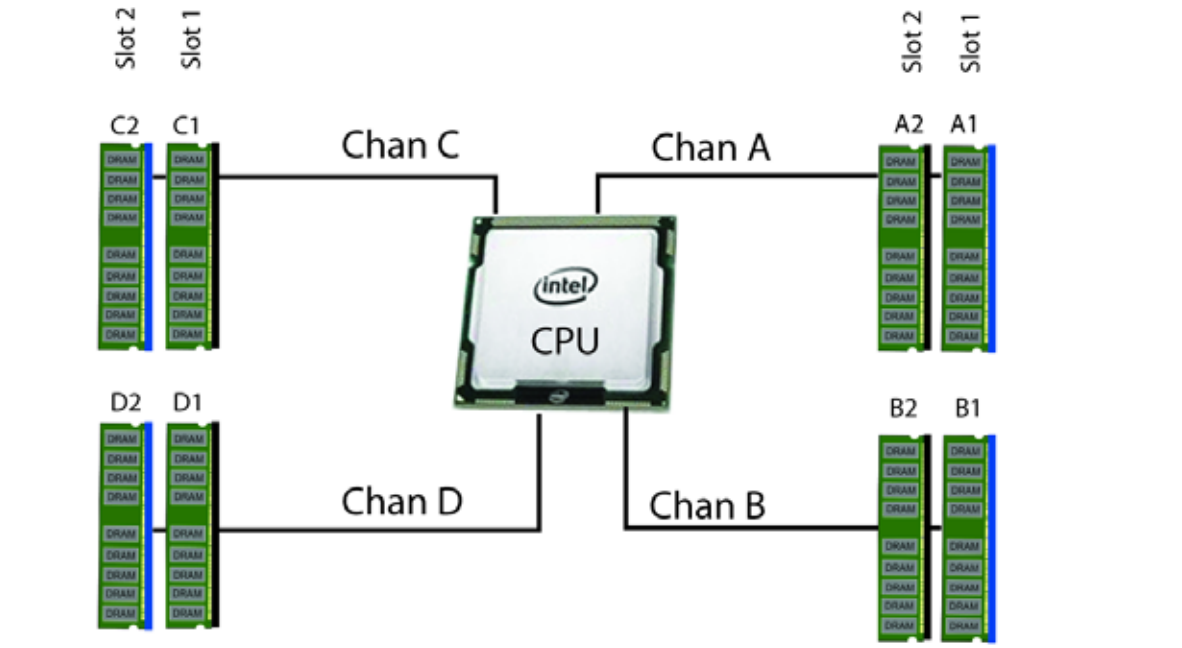
CHAPTER 1 MEMORY ORGANIZATION CAPABILITIES AND FEATURE

The ***Table 1.0*** below describes the main memory DIMM features supported on Cisco Unified Edge M8 Compute Node servers.

Table 1 Main Memory Features for RDIMM

Memory DIMM Server Technologies	Cisco Unified Edge M8 Compute Node
CPU Sockets	**Single-Socket**
Intel® Xeon® CPU generation	Intel® Xeon® 6 SoC with P-Cores Processor
DDR5 memory clock speed	Intel® Xeon® 6 SoC CPU: Up to 5600 MT/s 1DPC
Operational voltage	1.1 Volts
DRAM fab density	16Gb and 24Gb
Memory type	RDIMM (Registered DDR5 DIMM)
Memory DRAM DIMM organization	Four memory DIMM channels per CPU; up to 2 DIMMs Per Channel
Maximum number of DRAM DIMM per server	8 (1-Socket)
DRAM DIMM Densities and Ranks	16GB 1Rx8, 32GB 1Rx4, 48GB 1Rx4, 64GB 2Rx4, 96GB 2Rx4, 128GB 2Rx4
Maximum system memory capacity	1TB (8x128GB)

Figure 1 Single-socket memory organization block diagram



CHAPTER 2 MEMORY OPTIONS

- The available memory devices for Cisco Unified Edge M8 Compute Node are listed in ***Table 2.0***
- The memory PID decoder for Cisco Unified Edge M8 Compute Node Memory PIDs is shown in ***Table 2.1***

NOTE:

- When paired with Intel® Xeon® 6 SoC CPUs, all memory DIMMs must be Cisco DDR5-6400 memory PIDs, although the memory will operate at the maximum speed of the Intel® Xeon® 6 SoC CPUs memory controller, up to 5600 MT/s.

Table 2.0 Memory Options for UCS Cisco Unified Edge M8 Compute Node servers[1]

Memory DIMM Densities & Cisco PIDs	Memory DIMM Description	XE130c M8
DDR5-6400 MT/s Cisco Memory PIDs list		
16GB	16GB RDIMM 1Rx8 1.1Volts (16Gb)	UCSXE-MRX16G1RE5
32GB	32GB RDIMM 1Rx4 1.1Volts (16Gb)	UCSXE-MRX32G1RE5
48GB	48GB RDIMM 1Rx4 1.1Volts (24Gb)	UCSXE-MRX48G1RF5
64GB	64GB RDIMM 2Rx4 1.1Volts (16Gb)	UCSXE-MRX64G2RE5
96GB	96GB RDIMM 2Rx4 1.1Volts (24Gb)	UCSXE-MRX96G2RF5
128GB	128GB RDIMM 2Rx4 1.1Volts (32Gb)	UCSXE-MR128G2RG5

Notes:

1. Memory will operate at the maximum speed of the Intel® Xeon® 6 SoC CPUs memory controller, up to 5600 MT/s Check ***Table 6*** and ***Table 7*** for details on 1DPC and 2 DPC maximum speed with Intel® Xeon® 6 SoC CPUs.

Table 2.1 Memory PID Decoder

Identifier#1	Identifier#2	Identifier#3	Identifier#4	Identifier#5	Identifier#6	Identifier#7
Cisco Product Family	**Memory DIMM Type**	**DIMM Capacity (GB)**	**DIMM Org. (Rank)**	**DDR Generation & DRAM Density**	**DIMM Speed (Mega Transfers per second)**	**Option/Spare DIMM**
UCSXE	**MR**: RDIMM	X16G X32G X48G X64G X96G 128G	**1R:** Single-Rank **2R:** Dual-rank	**E:** DDR5/16Gb **F**: DDR5/24Gb G:DDR5/32Gb	5: 6400 MT/s	**Blank:** Option **=:** Spare

CHAPTER 3 DRAM GUIDELINES



GOLDEN RULE: Memory on every CPU socket shall be configured identically. Unbalanced populations are unsupported. Mixing different DIMM densities within the channel or across the channel is not supported.

- DIMM Count Rules:

Table 3 Allowed DIMM Count for 1-CPU[1]

Intel M8 Memory DIMM allowed counts	Memory DIMM description	1-CPU count
RDIMM		
16GB	16GB RDIMM 1Rx8	2,4,8
32GB	32GB RDIMM 1Rx4	2,4,8
48GB	48GB RDIMM 1Rx4	2,4,8
64GB	64GB RDIMM 2Rx4	2,4,8
96GB	96GB RDIMM 2Rx4	2,4,8
128GB	128GB RDIMM 2Rx4	2,4,8

Notes:

1. See ***Table 4*** for detailed populations and ***Table 5*.0** to ***Table 5*.1** for DIMM configurations.

- DIMM Population Rules:
  - Each channel has two memory slots (for example, channel A = slots A1 and A2). See **golden rule** above.
    - A channel can operate with one or two DIMMs installed.
    - If a channel has only one DIMM, populate slot 1 first (the blue slot).

Table 4 Intel SoC DIMM population order for 16GB, 32GB, 48GB, 64GB, 96GB, 128GB - up to 2DPC

# DIMMs per CPU	DIMM population - 64GB (Intel® Xeon® 6 SoC CPUs)	
	Slot 1 (Blue)	Slot 2 (Black)
2	A1, C1	-
4	A1, B1, C1, D1	-
8	A1, B1, C1, D1	A2, B2, C2, D2

- DIMM Mixing Rules:
  - All DIMMs must be DDR5-6400 DIMMs.
  - Mixing different DIMM densities in the same slot across channels is unsupported. All populated slots of the same color must have the same DIMM density.
  - Mixing different DIMM densities within the same channel is unsupported. Both slots of the same channel must have the same DIMM density.

- Mixing X4 and X8 DIMMs is not allowed in the same channel or across channels.
- Mixing 16Gb DRAM based with 24Gb DRAM based DIMMs is not allowed. Therefore, 48GB and 96GB cannot be mixed with any other memory DIMMs.
- Mixing 32Gb DRAM based with 24Gb or 16Gb DRAM based is not allowed. Therefore, 128GB cannot be mixed with any other memory DIMMs.
- The DIMM mixing rules matrix is described in the ***Table 5*.0 and *Table 5*.1** below.

Table 5.0 Supported DIMM mixing and population across 2 slots in each channel - 16Gb DRAM based DIMMs[1,2,3]

Channel Mixing		DIMM Slot 2 (Black)		
DIMM Slot 1 (Blue)		16GB	32GB	64GB
		1Rx8	1Rx4	2Rx4
16GB	1Rx8	Yes	No	No
32GB	1Rx4	No	Yes	No
64GB	2Rx4	No	No	Yes

Notes:
1. Mixing different DIMM densities in the same slot across channels is not supported.
2. All populated slots of the same color must have the same DIMM density.
3. 16Gb/32Gb/24Gb RDIMM mixing is not allowed.

Table 5.1 Supported DIMM mixing and population across 2 slots in each channel - 24Gb DRAM based DIMMs[1,2,3]

Channel Mixing		DIMM Slot 2 (Black)	
DIMM Slot 1 (Blue)		48GB	96GB
		1Rx8	1Rx4
48GB	1Rx8	Yes	No
96GB	1Rx4	No	Yes

Notes:
1. Mixing different DIMM densities in the same slot across channels is not supported.
2. All populated slots of the same color must have the same DIMM density.
3. 16Gb/32Gb/24Gb RDIMM mixing is not allowed.

- Memory Limitations:
  - Memory on every CPU socket shall be configured identically. See **golden rule from page 9**.
  - Refer to ***Table 4*, *Table 5.0* and *Table 5*.1** for DIMM population and DIMM mixing rules.
  - Cisco memory from previous generation servers (DDR5-4800 and DDR5-5600) is not supported with the Intel M8 servers.

Table 6 Maximum DIMM Memory Operating Frequency on Intel® Xeon® 6 SoC CPUs(1) for XE130c M8 Compute Node[1]

Intel® Xeon® 6 SoC CPU Memory Speed - Cisco Unified Edge M8 Compute Node	1DPC	2DPC
	All RDIMMs	All RDIMMs
Intel® Xeon® 6 SoC 6543P-B and 6513P-B CPU	5600 MT/s	5200 MT/s
Intel® Xeon® 6 SoC 6503P-B CPU	4800 MT/s	4800 MT/s

Notes:

1. Memory will operate at the maximum speed of the Intel® Xeon® 6 SoC CPUs memory controller, up to 5600 MT/s.

Table 7 Maximum DIMM Memory Operating Frequency on Intel® Xeon® 6 SoC CPUs(1) for XE150C M8 Compute Node[1]

Intel® Xeon® 6 SoC CPU Memory Speed - XE150C M8 compute Node	1DPC	2DPC
	All RDIMMs	All RDIMMs
Intel® Xeon® 6 SoC 6544P-B and 6513P-B CPU	5600 MT/s	5200 MT/s

Notes:

1. Memory will operate at the maximum speed of the Intel® Xeon® 6 SoC CPUs memory controller, up to 5600 MT/s.

CHAPTER 4 SUPPORTED DRAM DIMM CONFIGURATIONS

Table 8, below, shows the supported DIMM configurations with 2, 4, and 8 DIMMs per CPU.

Table 8 Supported DIMM Configurations for Intel® Xeon® 6 SoC Scalable Processors

DDR5 Memory Total System Capacity	Capacity Per CPU (GB)		Total DIMMs Per CPU
1-CPU	Blue Slots A1 to D1	Black Slots A2 to D2	
16GB RDIMMs			
32GB	2x16GB	-	2
64GB	4x16GB	-	4
128GB	4x16GB	4x16GB	8
32GB RDIMMs			
64GB	2x32GB	-	2
128GB	4x32GB	-	4
256GB	4x32GB	4x32GB	8
48GB RDIMMs			
96GB	2x48GB	-	2
192GB	4x48GB	-	4
384GB	4x48GB	4x48GB	8
64GB RDIMMs			
128GB	2x64GB	-	2
256GB	4x64GB	-	4
512GB	4x64GB	4x64GB	8
96GB RDIMMs			
192GB	2x96GB	-	2
386GB	4x96GB	-	4
768GB	4x96GB	4x96GB	8
128GB RDIMMs			
256GB	2x128GB	-	2
512GB	4x128GB	-	4
1024GB	4x128GB	4x128GB	8

CHAPTER 5 INSTALLING a DIMM or DIMM BLANK

To install a DIMM or a DIMM blank into a slot on the blade server, follow these steps.

Procedure

Step 1 Open both DIMM connector latches.

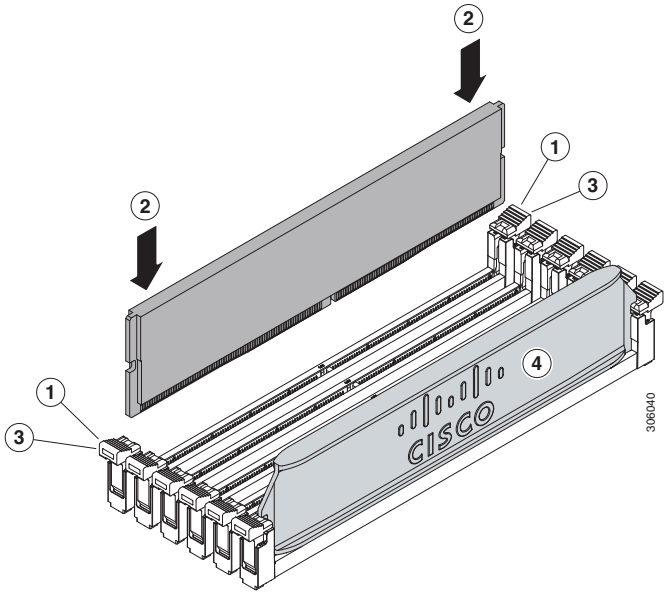
Step 2 Press evenly on both ends of the DIMM until it clicks into place in its slot

Note: Ensure that the notch in the DIMM aligns with the slot. If the notch is misaligned, it is possible to damage the DIMM, the slot, or both.

Step 3 Press the DIMM connector latches inward slightly to seat them fully.

Step 4 Populate all slots with a DIMM or DIMM blank. A slot cannot be empty.

Figure 2 Installing Memory



Change log

Please find the below table for the recent changes happened in the document.

Table 9 Change log

Publication Date	Revision
02/24/2025	Initial Memory Guide set up is completed
04/01/2026	XE150c is added to the memory guide

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